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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,920	02/02/2001	James J. Alwan	100.718.419 (MIC- 77US)	8909

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EXAMINER	
MACCHIAROLO, PETER J	
ART UNIT	**PAPER NUMBER**
2879	

DATE MAILED: 06/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/775,920	ALWAN, JAMES J.	
	Examiner	Art Unit	
	Peter J Macchiarolo	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The reply filed on 05/12/2004 consists of changes to the specification, drawings, and to the claims, and further, the reply consists of remarks related to the prior rejection of claims in the previous Office Action. In light of the remarks and arguments, the finality of the previous office action is hereby withdrawn, and an action on the merits follows. Pending claims 13-26 are not allowable as explained below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 13-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of previously cited Sandhu et al (USPN 5271798; "Sandhu") in further view of Potter (USPN 5700176; "Potter").

3. In regards to claims 13-21, and 24, Applicant admits the prior art includes a method of forming an FED comprising providing a substrate having a central area and a peripheral area, forming alignment marks on the peripheral area of the substrate, forming an emitter electrode structure on the central area of the substrate, forming a plurality of micropoints in groups on the emitter electrode structure, depositing an insulating layer over the substrate, emitter electrode structure, and plurality of micropoints, and depositing a conductive layer over the insulating

layer. Applicant further admits it is known that selectively etching openings through the conductive and insulating layers comprises applying a layer of photoresist on said conductive layer, imaging said photoresist to define a pattern for said openings, developing the photoresist, and etching the pattern for the openings. The Examiner further notes this is a well known method of manufacture.

4. Applicant further admits a method of making a semiconductor wafer to clear alignment marks by locally applying a wet etchant to uncover a structure is known in the art to effectively clear the marks without the use of photolithography[1] (see also Sandhu).

5. Neither Sandhu nor Applicant discloses that the semiconductor manufacturing method comprising selectively spraying a wet etchant on a structure can be used for FED fabrication.

6. However, Potter teaches a process for producing field emission devices are generally more attractive alternatives to semiconductor devices for many applications, being capable of high performance and being capable of fabrication from a wide range of materials with less stringent controls of material purity, but with fabrication processes and equipment similar to those used for semiconductor fabrication.[2] Further, Potter shows in figure 1, a cathode (100) and an anode (70) assembly assembled together in a FED, which can be automatically aligned, or aligned according to the well-known prior art method i.e. with alignment marks. Potter further teaches contact pads are selectively provided at the device top surface to make electrical contact, which may require the same clearing method as described in Sandhu.

7. Therefore, in view of the above discussion, it would have been obvious to one having ordinary skill in the art at the time the invention was made to construct an FED with the method

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[1] Instant spec., page 4, para. 2.

admitted by Applicant and Sandhu to allow for less pure materials and cheaper manufacturing method.

8. In regards to claims 22, 23, 25 and 26, Applicant admits the prior art includes a method of forming a cathode assembly of a field emission device comprising providing a substrate, making alignment marks in a peripheral region of the substrate, forming an emitter electrode structure on a central region of the substrate, said central region being substantially surrounded by the peripheral region, forming a plurality of micropoints on the emitter electrode structure, depositing an insulating layer over the substrate, emitter electrode structure, and plurality of micropoints, depositing a first conductive layer over the insulating layer, polishing the conductive layer via chemical-mechanical planarization, and etching openings through the conductive and insulating layers to expose the micropoints, with walls defining the openings being spaced away from the micropoints. The Examiner further notes this is a well-known method of manufacturing in the art of FED's.

9. Applicant further admits a method of making a semiconductor wafer to clear alignment marks by locally applying a wet etchant to uncover a structure is known in the art to effectively clear the marks without the use of photolithography[3] (see also Sandhu).

10. Neither Sandhu nor Applicant discloses that the semiconductor manufacturing method comprising selectively spraying a wet etchant on a structure can be used for FED fabrication.

11. However, in view of Potter's teaching and the above discussion and, it would have been obvious to one having ordinary skill in the art at the time the invention was made to construct an

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[2] Potter, abstract, and col. 23-29.

FED with the method admitted by Applicant and Sandhu to allow for less pure materials and cheaper manufacturing method.

Response to Arguments

12. Applicant's arguments filed 05/12/2004 have been fully considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. Spindt et al. ("Physical properties of thin-film field emission cathodes with molybdenum cones," Journal of Applied Physics (USA), vol. 47, no. 12, p. 5248-63, Dec. 1976) is further evidence a semiconductor manufacturing method can be used for FED fabrication.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter J Macchiarolo whose telephone number is (571) 272-2375. The examiner can normally be reached on 8:30 - 5:00, M-F.

16. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar Patel can be reached on (571) 272-2475. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

17. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

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[3] Instant spec., page 4, para. 2.

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

pjm

ASHOK PATEL
PRIMARY EXAMINER